TSMC-00-068BD

April 5, 2004

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/790,919 03/02/04
Ta-Lee Yu
BIPOLAR ESD PROTECTION STRUCTURE

INFORMATION DISCLOSURE STATEMENT

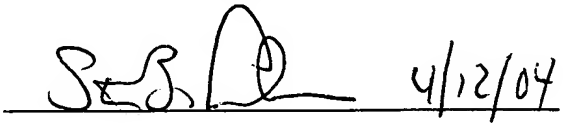
Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on April 12, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date  4/12/04

The report by J. Chen et al., "Design and Layout of a High ESD Performance NPN Structure for Submicron BiCMOS/Bipolar Circuits," IEEE Journal 1996, 0-7803-2753-5/96, pp. 227-232, describes how ESD efficiency is typically measured by dividing the ESD "threshold" voltage by the area of the ESD protection device and discusses various ESD protection device layouts.

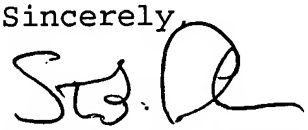
U.S. Patent 5,850,095 to Chen et al., "ESD Protection Circuit Using Zener Diode and Interdigitated NPN Transistor," describes an electrostatic discharge (ESD) protection circuit.

U.S. Patent 5,341,005 to Canclini, "Sturcture for Protecting an Integrated Circuit from Electrostatic Discharges," discloses different structures for ESD protection.

U.S. Patent 5,528,189 to Khatibzadeh, "Noise Performance of Amplifiers," discloses an amplifier with ESD protection with emitter finger layouts.

U.S. Patent 5,301,084 to Miller, "Electrostatic Discharge Protection for CMOS Integrated Circuits," discusses ESD protection circuits.

Sincerely,



Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

OIPE APR 15 2004 PATENT & TRADEMARK OFFICE

Docket Number (Optional)	Application Number
TSMC-00-0688D	10/790,919
Applicant: Ta Lee Yu	
Filing Date: 03/02/04	Group Art Unit:

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
	5850095	12/15/98	Chen et al.	257	361	9/24/96
	5341005	8/23/94	Canclini	257	173	9/8/92
	5528189	6/18/96	Khatibzadeh	327	314	12/21/93
	5301084	4/5/94	Miller	361	91	8/21/91

FOREIGN PATENT DOCUMENTS

	Document Number	Date	Country	Class	Subclass	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

- J. Chen et al., "Design and Layout of a High ESD Performance NPN Structure for Submicron BiCMOS/Bipolar Circuits", IEEE Jrnl 1996, 0-7803-2753-5/96, pp. 227-232.

Examiner	Date Considered

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.